IT IS CLAIMED:

1. A mass storage system for use with a computer system, comprising:

a plurality of solid-state memory device chips, each having a large number of memory cells partitioned into individually addressable chunks for write or read operations, said memory cells being organized into one or more sectors individually addressable for erase operation;

a memory chip controller for controlling the plurality of memory chips, said memory chip controller being adapted to communicate with the computer system; and

a device bus for connecting said memory chip controller to each of said plurality of solid-state memory chips, said device bus carrying serialized address, data and command information, thereby substantially reducing the number of connections therebetween.

2. A mass storage system as in claim 1, wherein the memory chips are flash EEPROM devices.

3. A mass storage system as in claim 1, wherein the device bus includes two serial-in lines, two serial-out lines, a clock line, a master chip-select line, a serial protocol control line, and a plurality of power lines.

4. A mass storage system as in claim 3, wherein the memory chips are flash EEPROM devices.

5. A mass storage system as in claim 1, wherein the device bus consists of two serial-in lines, two serial-out lines, a clock line, a master chip-select line, a serial protocol control line, and a plurality of power lines.

6. A mass storage system as in claim 5, wherein the memory chips are flash EEPROM devices.

7. A mass storage system as in claim 1, wherein the mass storage system is adapted to communicate with the computer system via a standard computer system bus, and wherein the mass storage system is adapted to be powered by a standard power supply within the computer system.

8. A mass storage system as in claim 7, wherein the memory chips are flash EEPROM devices.

9. A mass storage system as in claim 1, wherein the mass storage system is adapted to communicate with the computer system via a standard computer bus interface, and wherein the mass storage system is adapted to be powered by a standard power supply within the computer system.

10. A mass storage system as in claim 9, wherein the memory chips are flash EEPROM devices.

11. A mass storage system as in claim 1, further including:

one or more backplanes each containing a plurality of mounts, each said plurality of mounts adapted to receive one of the plurality of memory chips;

an extension of the device bus to each of the plurality of mounts for connection to the memory chip thereon;

a set of device-select pinouts on each memory chip;

a set of corresponding pads on each mount for connection to the set of device-select pinouts of the memory chips mounted thereon, said set of corresponding pads having a predetermined configuration of grounded pads to define a mount address and therefore a unique array address for each memory chip mounted on each said one or more backplanes.

12. A mass storage system as in claim 11, wherein the memory chips are

flash EEPROM devices.

13. A mass storage system as in claim 11, each said memory chip further including:

a device select circuit for enabling the memory chip thereof whenever ap array address received from the device bus coincides with the array address obtained from the set of device-select pinouts as defined by the predetermined configuration of grounded bonding pads.

14. A mass storage system as in claim 13, wherein the memory chips are flash EEPROM devices.

15. A mass storage system as in claim 13, said device select circuit further including:

means responsive to an asserting chip-select signal and a clock signal from the device bus for converting a serialized array address from the device bus to a corresponding parallel array address; and

means for asserting a memory chip-select signal whenever a match occurs between the corresponding parallel array address and the array address obtained from the set of device-select pinouts as defined by the predetermined configuration of grounded bonding pads.

16. A mass storage system as in claim 15, wherein the memory chips are flash EEPROM devices.

17. A mass storage system as in claim 13, wherein said device select circuit further including:

a master-select circuit for enabling the memory chip thereof whenever said set of corresponding pads are configured with a predetermined, master-select grounding configuration.

18. A mass storage system as in claim 17, wherein the memory chips are flash EEPROM devices.

19. A mass storage system as in claim 17, wherein the memory chip is enabled by said master-select circuit and a dedicated chip select signal.

20. A mass storage system as in claim 19, wherein the memory chips are flash EEPROM devices.

21. A mass storage system as in claim 11, wherein said device select circuit further including:

a device deselect circuit for disabling each memory chip thereof whenever an array address received from the device bus coincides with a predetermined address.

22. A mass storage system as in claim 21, wherein the memory chips are flash EEPROM devices.

23. A mass storage system as in claim 1, further including:

one or more memory submodules each containing a plurality of memory-device mounts, each memory-device mount adapted to receive one of the plurality of memory chips;

one or more backplanes each containing a plurality of submodule mounts adapted to receive one of the plurality of memory submodules;

an extension of the device bus to each memory submodule for connection to each memory-device mount and therefore to each memory chip thereon;

a set of device-select pinouts on each memory chip;

a set of corresponding pads on each memorydevice mount for connection to the set of device-select pinouts of the memory chips mounted thereon, said set of corresponding pads being partitioned into first and second subsets of pads;

said first subset of pads capable of providing group of grounded pads

configurations to define unique addresses for all memory-device mounts and therefore addresses for corresponding memory chips mounted on each memory submodule; and

said second subset of pads being connected to corresponding pads on each submodule mount and capable of providing a second group of grounded pads configurations to define unique addresses for all submodule mounts and therefore addresses for corresponding memory submodules mounted on each backplane.

24. A mass storage system as in claim 23, wherein the memory chips are flash EEPROM devices.

25. A mass storage system as in claim 23, each said memory chip further including:

a device select circuit for enabling the memory chip thereof whenever an array address received from the device bus coincides with the array address obtained from the set of device-select pinouts as defined by the predetermined configuration of grounded bonding pads.

26. A mass storage system as in claim 25, wherein the memory chips are flash EEPROM devices.

27. A mass storage system as in claim 25, said device select circuit further including:

means responsive to an asserting chip-select signal and a clock signal from the device bus for converting a serialized array address from the device bus to a corresponding parallel array address; and

means for asserting a memory chip-select signal whenever a match occurs between the corresponding parallel array address and the array address obtained from the set of device-select pinouts as defined by the predetermined configuration of grounded bonding pads.

28. A mass storage system as in claim 27, wherein the memory chips are

flash EEPROM devices.

29. A mass storage system as in claim 25, wherein said device select circuit further including: a master-select circuit for enabling the memory chip thereof whenever said set of corresponding pads are configured with a predetermined, master-select grounding configuration.

30. A mass storage system as in claim 29, wherein the memory chips are flash EEPROM devices.

31. A mass storage system as in claim 29, wherein the memory chip is enabled by said master-select circuit and a dedicated chip select signal.

32. A mass storage system as in claim 31, wherein the memory chips are flash EEPROM devices.

33. A mass storage system as in claim 23, wherein said device select circuit further including:

a device deselect circuit for disabling each memory chip thereof whenever an array address received from the device bus coincides with a predetermined address.

34. A mass storage system as in claim 33, wherein the memory chips are flash EEPROM devices.

35. A mass storage system as in claim 1, each said solid-state memory device further including:

a serial protocol logic for controlling the protocol of the serialized address, data and command information carried in the device bus, said serial protocol logic comprising;

means for routing and converting serialized addresses from the device bus to a

parallel address bus; means for routing and converting serialized data from the device bus to a parallel data bus;

means for routing and converting serialized command codes from the device bus to a plurality of parallel command lines;

a pointer shift register means for capturing a code from the device bus;

a pointer decode means for selectively enable said one of the routing and converting means; and

a serial protocol control signal from the device bus for enabling said pointer shift register means for capturing the code from the device bus while disabling said converting means, and for disabling said pointer shift register means after the code has been captured and enabling said routing and converting means.

36. A mass storage system as in claim 35, wherein the memory chips are flash EEPROM devices.

37. A method for transferring command, address and data information between two system via a serial bus connected therebetween, comprising the steps of:

serializing each command, address or data information into respective string components;

providing a code tag to each respective string component;

multiplexing the respective string components into a serial stream so that each respective string component has a definite start and end time sequence and is preceded by its corresponding tag code;

providing a serial protocol control signal which provides a time reference for the start and end of each respective string component in the serial stream;

transferring the serial stream and the serial protocol control signal from one system to another system;

detecting the start and end of each respective string component in the serial stream by reference to the serial protocol control signal;

reading the tag code of each respective string component and routing each respective string component in the serial stream accordingly, thereby extracting each command, address or data string components from the serial stream in the other system.

38. A method as in claim 37, further comprising the step of:

converting each routed command, address and data information back to a parallel format.

39. In a memory system having at least one memory device in communication with a controller, said memory device transferring data with the controller serially, an improved method of reading data stored in the memory device, comprising the steps of:

reading a new chunk of data as a current chunk of data from the memory device in parallel;

converting the current chunk of read data from parallel to serial format and shifting out to the controller;

setting up the address for the next chunk of data to be read and sending it from the controller to the memory device while the current chunk of data is being shifted out from the memory device to the controller;

accessing the memory device with the address for the next chunk of data while the current chunk of data is being shifted out from the memory device to the controller; and

repeating all the above steps, after the current chunk has been shifted out of the memory device, until all chunks to be read have been shifted out of the memory device.